Claims

1. A current conveyor circuit capable of operating at very low voltages, said circuit comprising: three LVCM's and four MOSFETS, wherein LVCM1 provides a constant bias current to flow through M3, if port X is kept open and the difference between the bias current and the injected current flows through M3 if a current is injected into port X, which gets reflected at port Z due to the action of LVCM1, M3 and M4, LVCM2 maintains the drain currents of M1 and M2 constant, and LVCM3 maintains a constant tail current in the circuit.

2. A circuit as claimed in claim 1, wherein the current conveyor comprises of one PMOS LVCM.

3. A circuit as claimed in claim 1, wherein LVCM2 is a PMOS LVCM.

4. A circuit as claimed in claim 1, wherein the current conveyor comprises of two NMOS LVCM's.

5. A circuit as claimed in claim 1, wherein LVCM1 is a single input, double output NMOS LVCM.

6. A circuit as claimed in claim 1, wherein LVCM2 is a single input single output NMOS LVCM.

7. A circuit as claimed in claim 1, wherein the LVCM uses the conventional CM structure in conjunction with a level shifter transistor at the input port.

8. A circuit as claimed in claim 1, wherein the LVCM imparts high swing capability.

9. A circuit as claimed in claim 1, wherein the LVCM's ensure maximum possible input and output voltage swings, giving rise to rail to rail capability to voltage transfer blocks.

10. A circuit as claimed in claim 1, wherein adaptive biasing technique is used in the LVCM.

11. A circuit as claimed in claim 1, wherein the adaptive biasing technique increases the input voltage swing and decreases the offset current.

12. A circuit as claimed in claim 1, wherein the MOSFET's M1 and M2 form a differential pair.

13. A circuit as claimed in claim 1, wherein the voltage at port voltage at port Y gets transferred to port X due to the action of the differential pair.

14. A circuit as claimed in claim 1, wherein the current conveyor may further comprise of a capacitance C connected between the drain of M1 and gate of M2.

15. A circuit as claimed in claim 1, wherein the capacitance is connected to provide compensation.

16. A circuit as claimed in claim 1, wherein the current conveyor may further comprise of a resistance connected between the gate terminal of M1 and M2.

17. A circuit as claimed in claim 1, wherein the resistance enhances the frequency response of the circuit.

18. A circuit as claimed in claim 1, wherein the MOSFET's M3 and M4 form a current mirror.

19. A circuit as claimed in claim 1, wherein the current conveyor operates at a voltage range of ± 1V.